

Fig. 1

*Microprocessor with BTAC Write Queue*

100

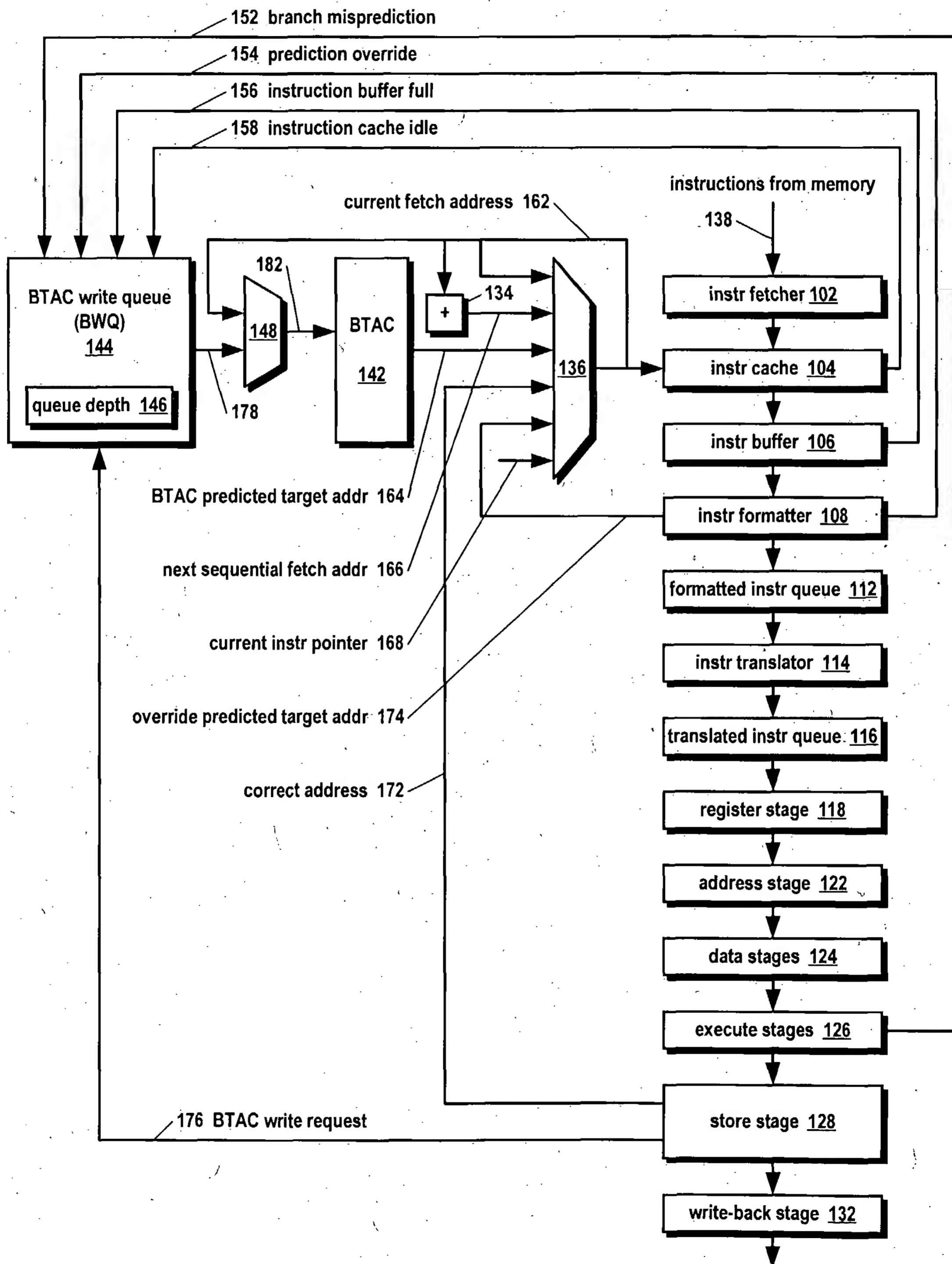


Fig. 2

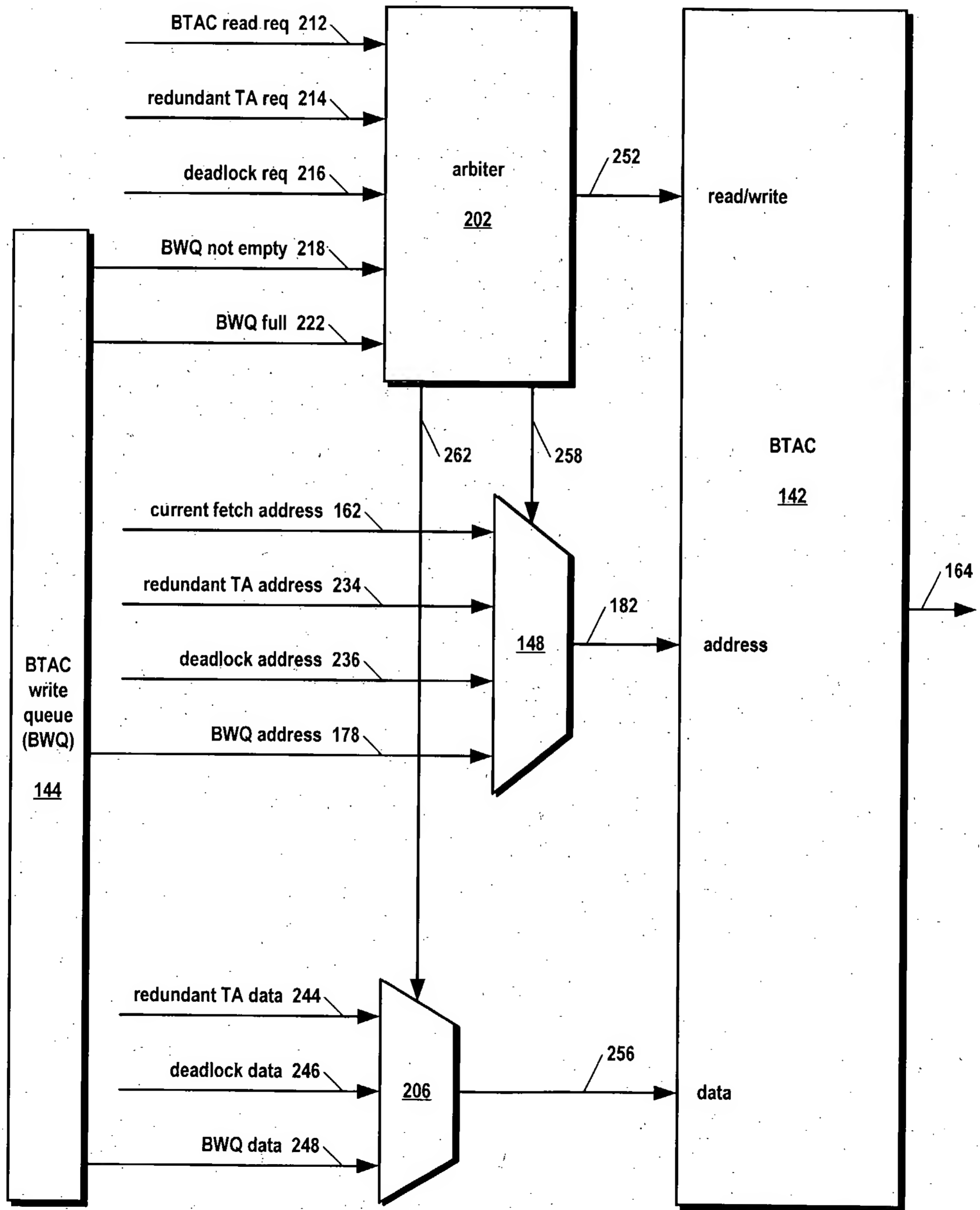
*Microprocessor with BTAC Write Queue*

Fig. 3

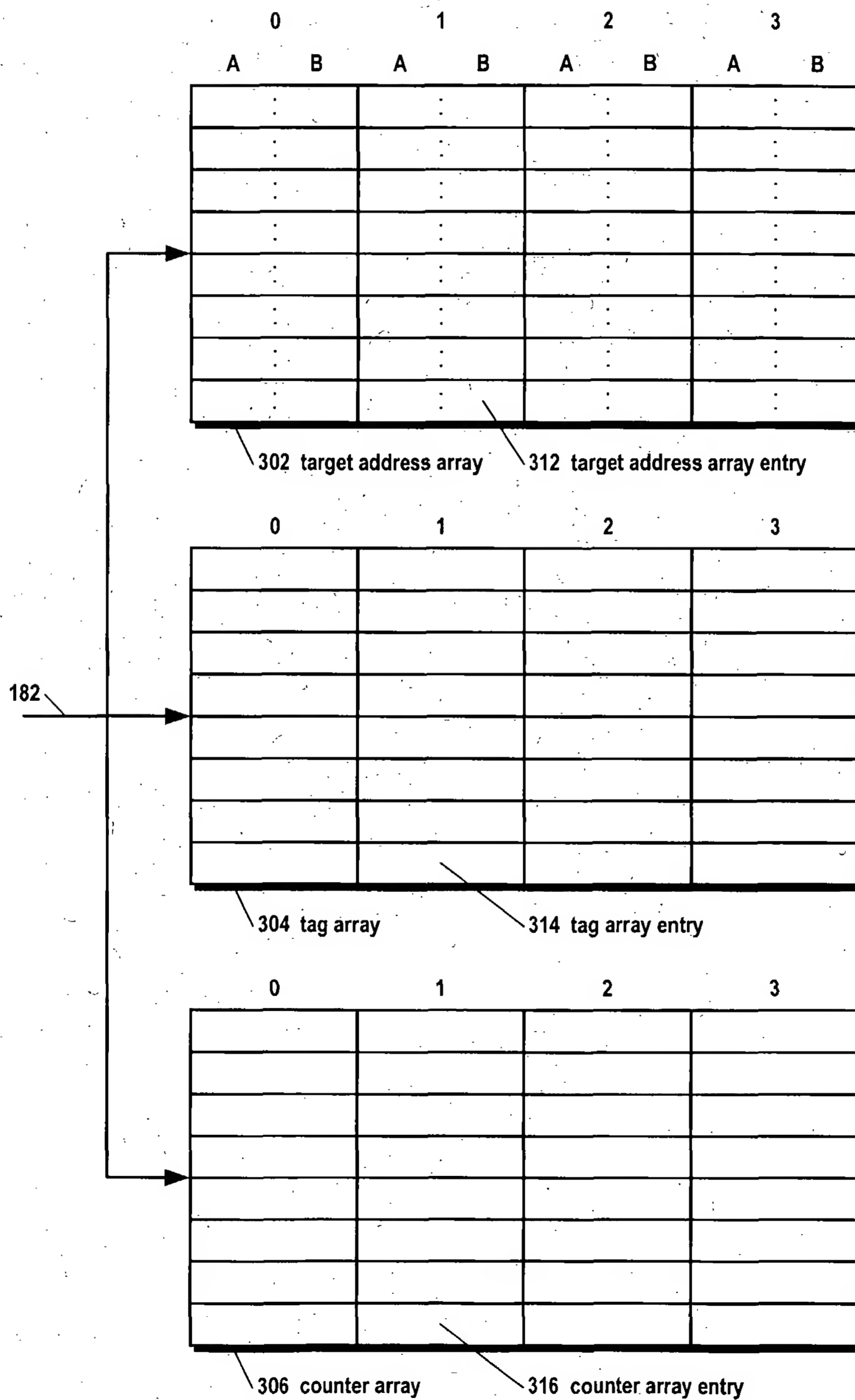
BTAC Arrays

Fig. 4

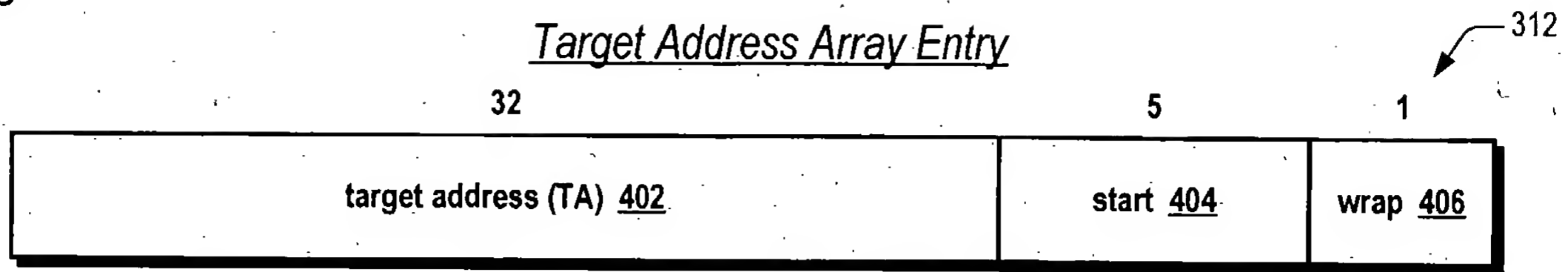


Fig. 5

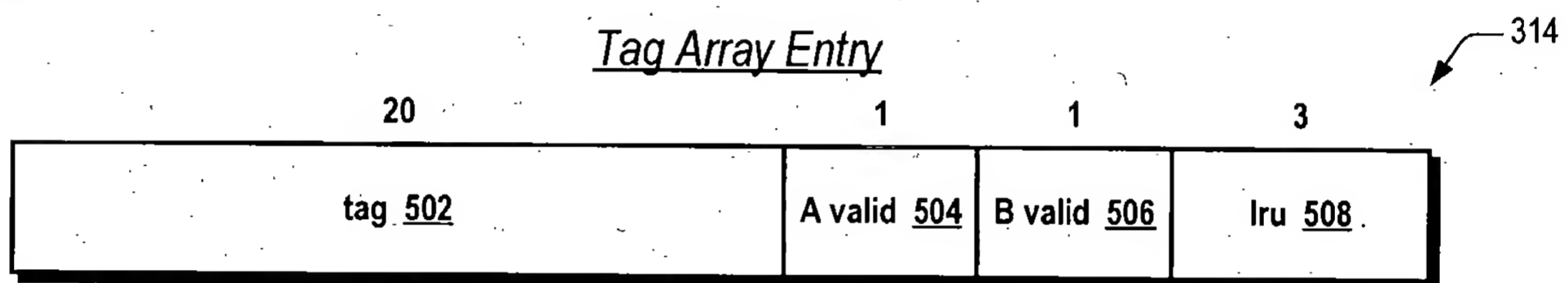


Fig. 6

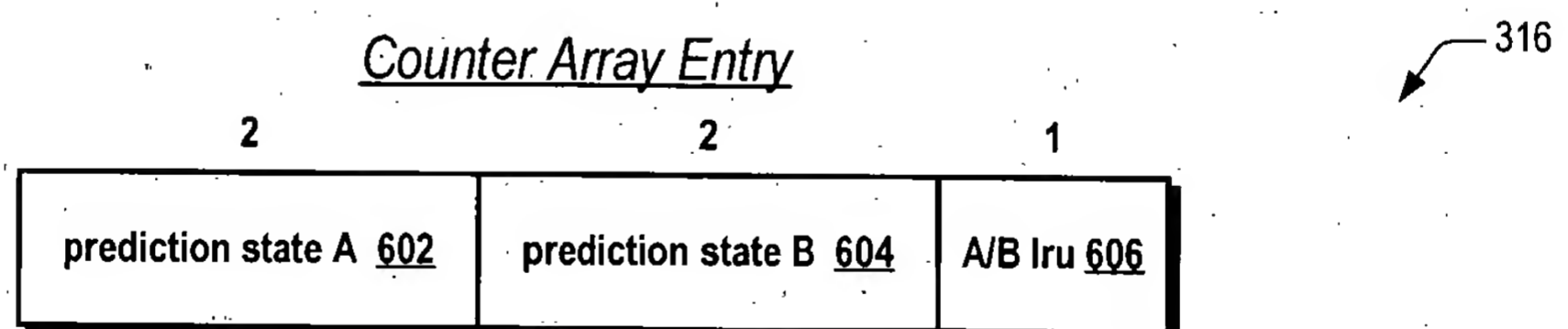


Fig. 7

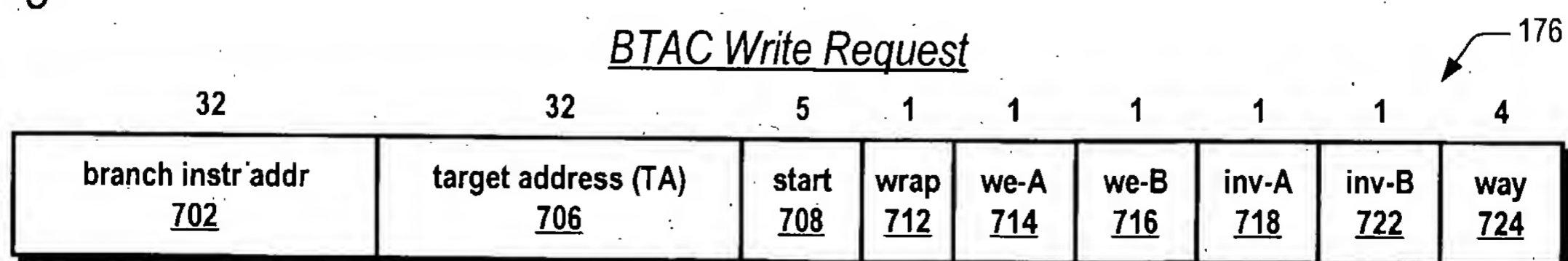




Fig. 9

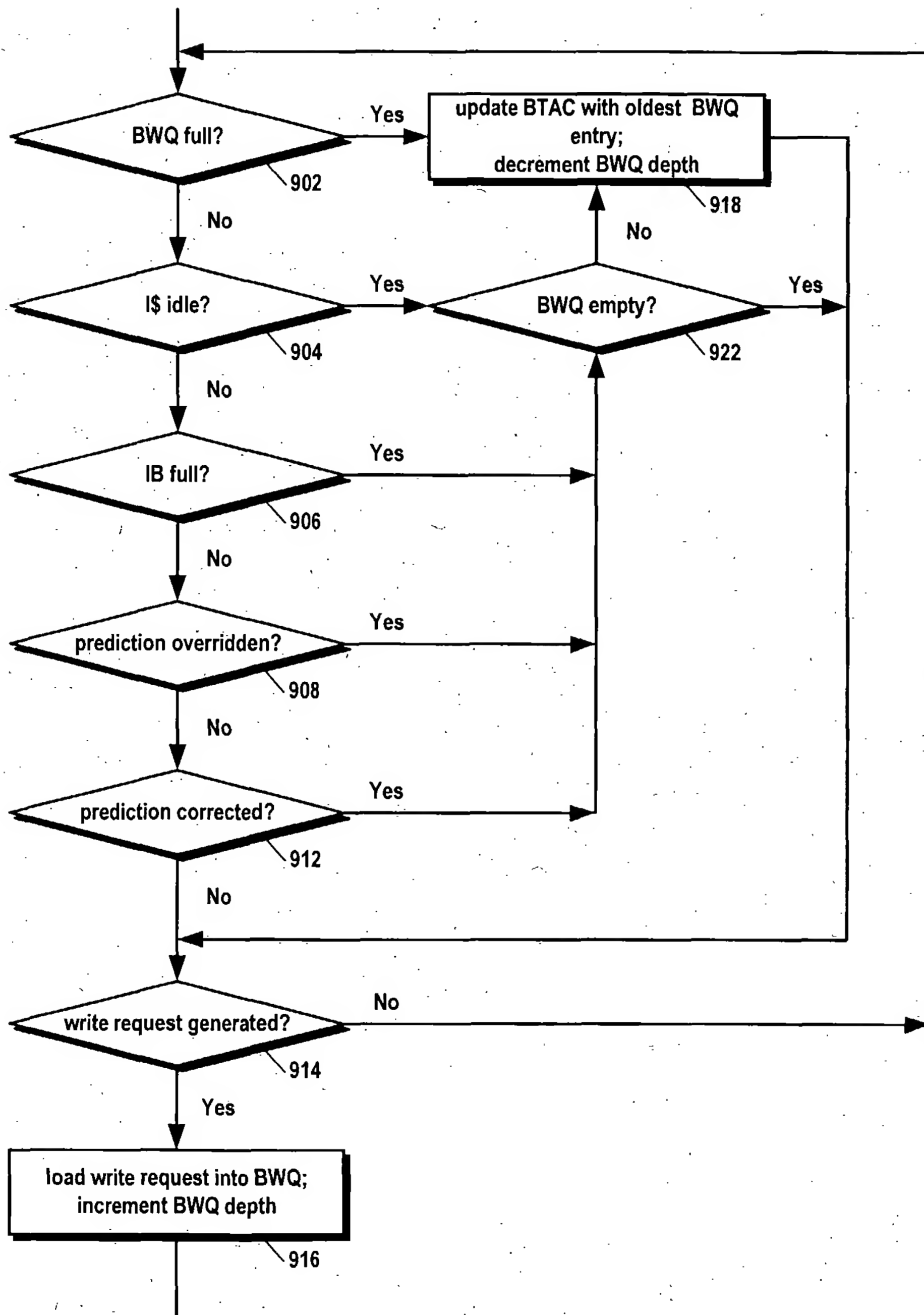
BTAC Write Queue Operation

Fig. 10

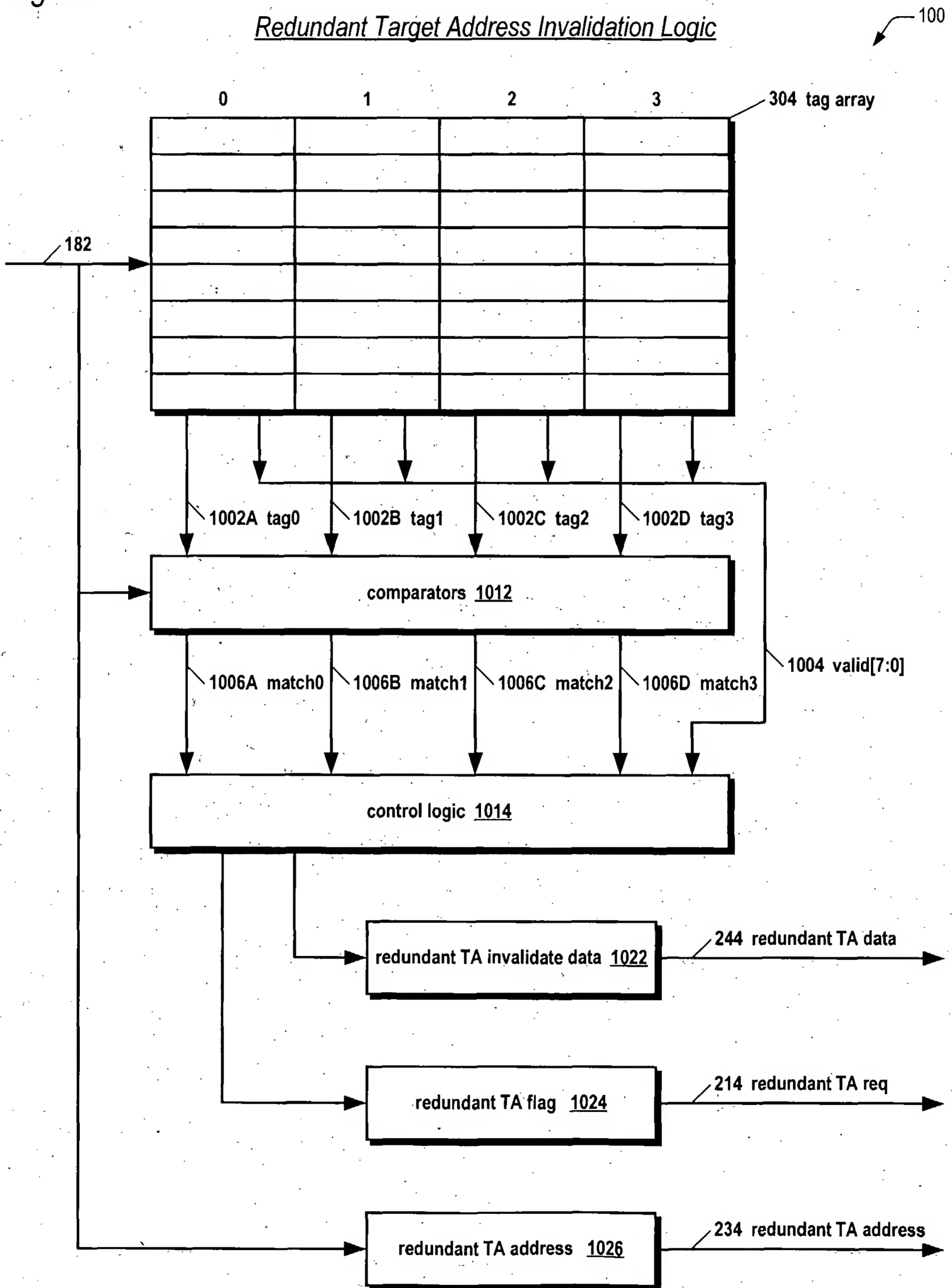


Fig. 11

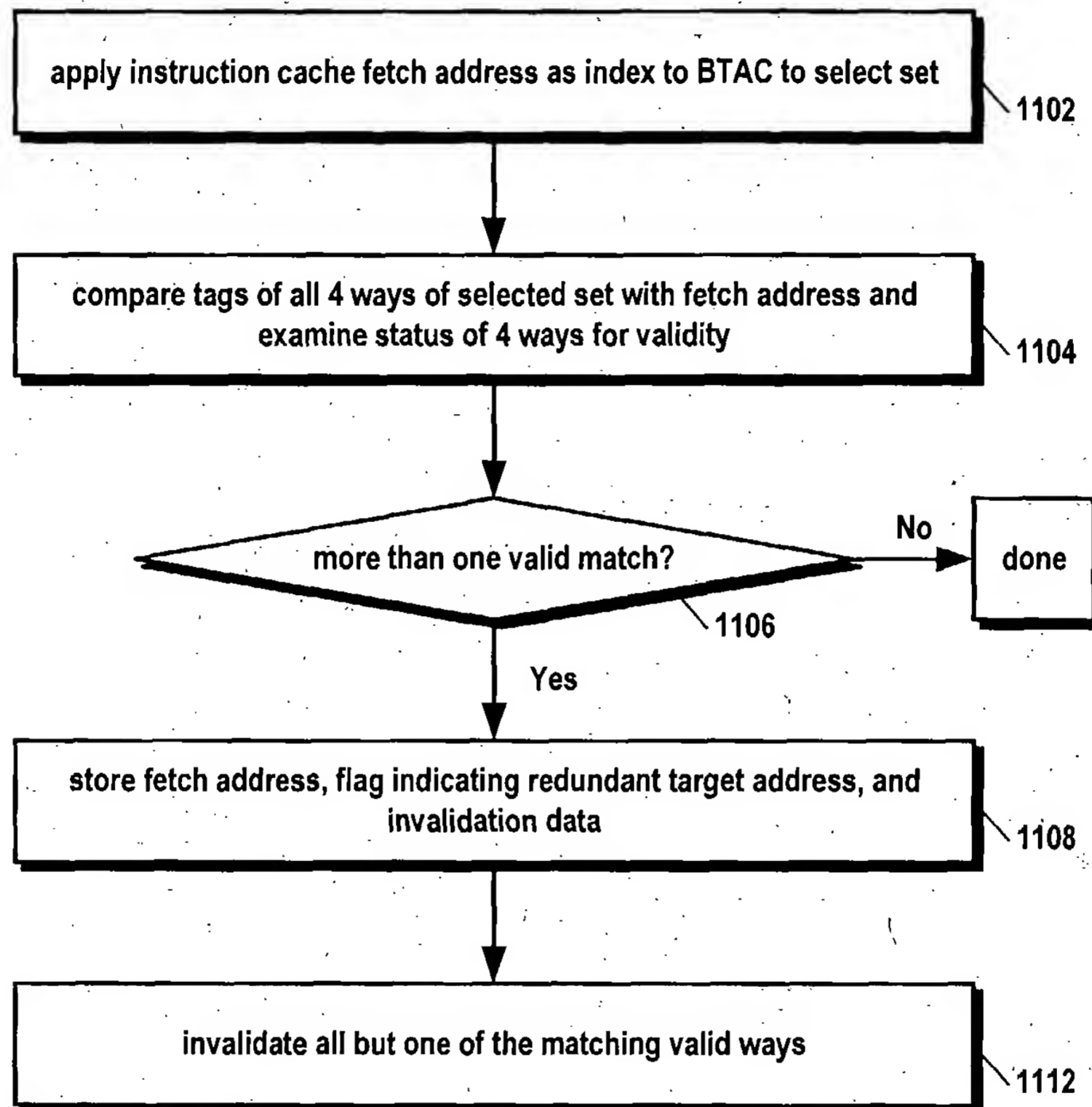
Redundant Target Address Invalidation Operation

Fig. 12

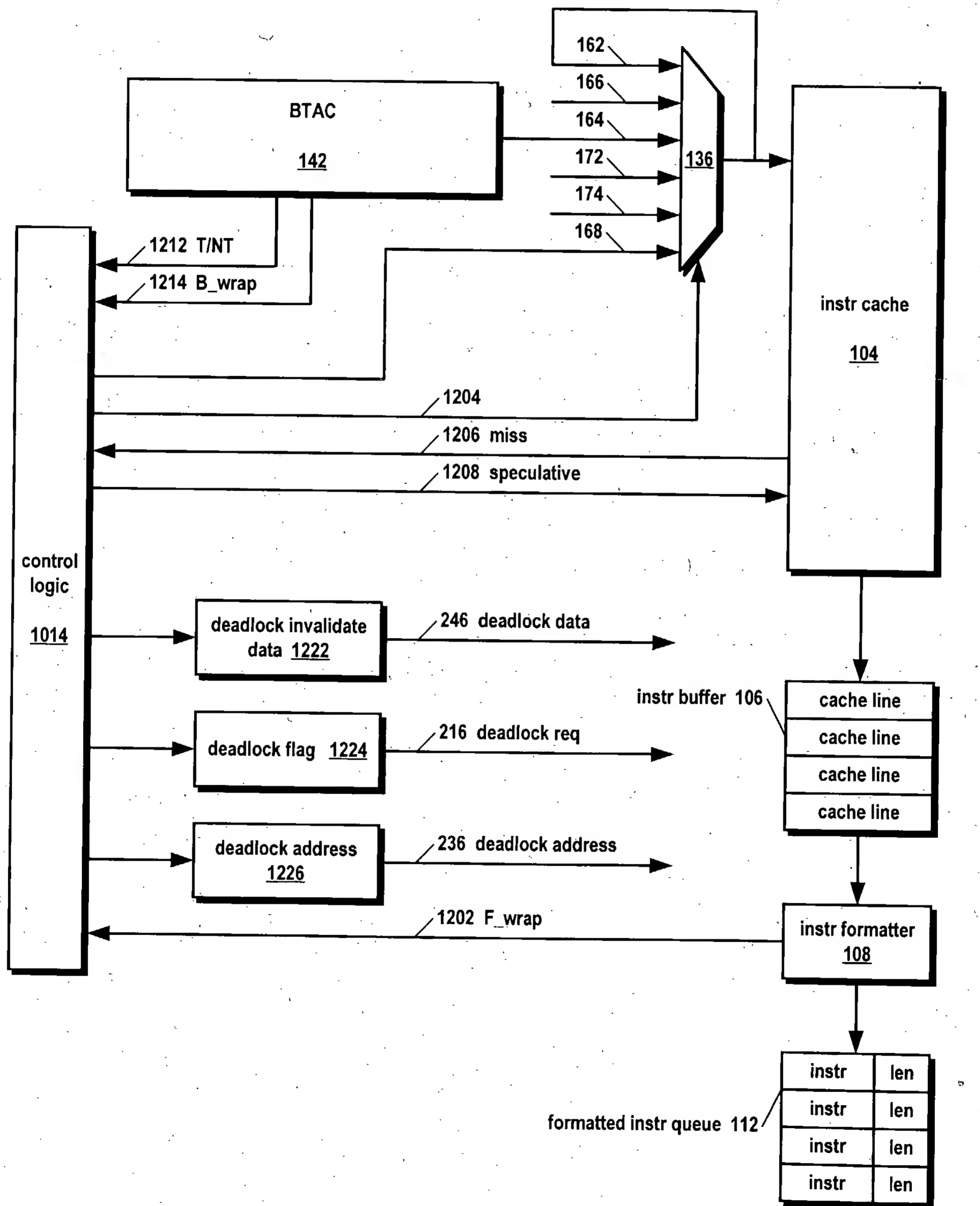
*Deadlock Resolution Apparatus*

Fig. 13

Deadlock Resolution Apparatus Operation